EE 435

Lecture 26

Data Converter Performance Characterization

Review from last lecture

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Review from last lecture

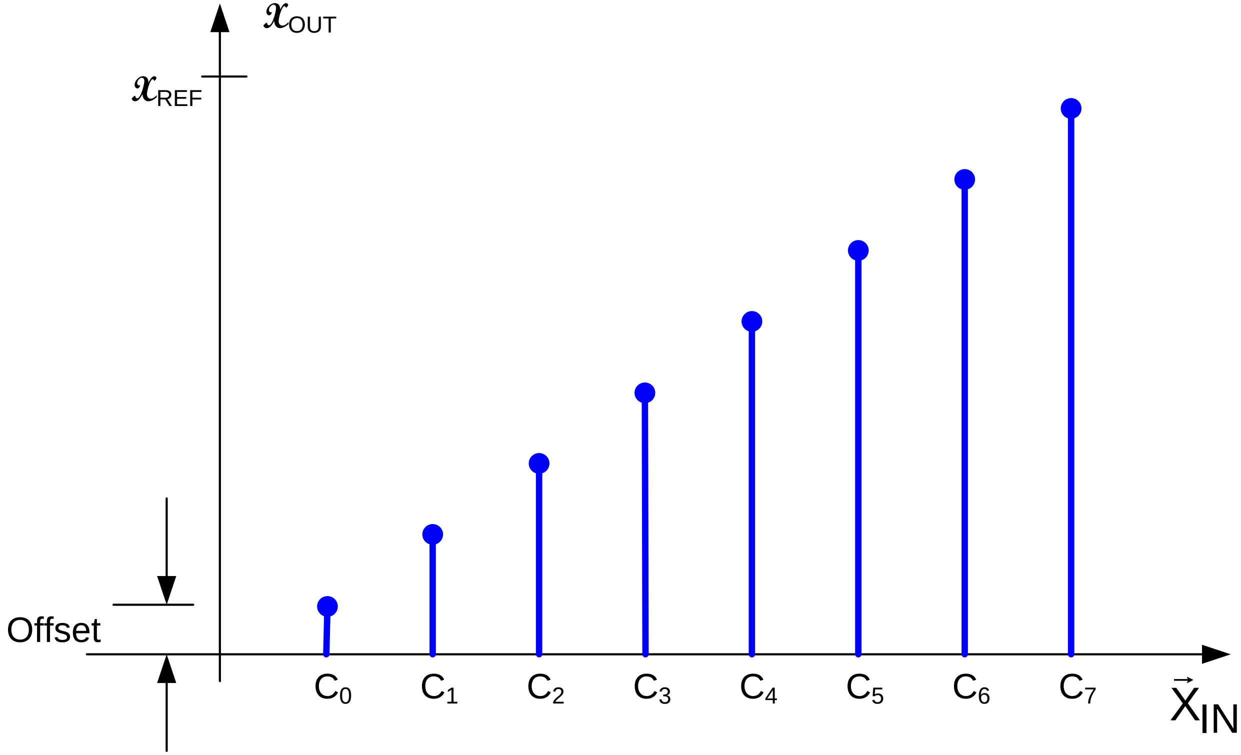
Performance Characterization of Data Converters

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

Review from last lecture

Performance Characterization

Offset (for DAC)



- Offset strongly (totally) dependent upon performance at a single point
- Probably more useful to define relative to a fit of the data

Review from last lecture

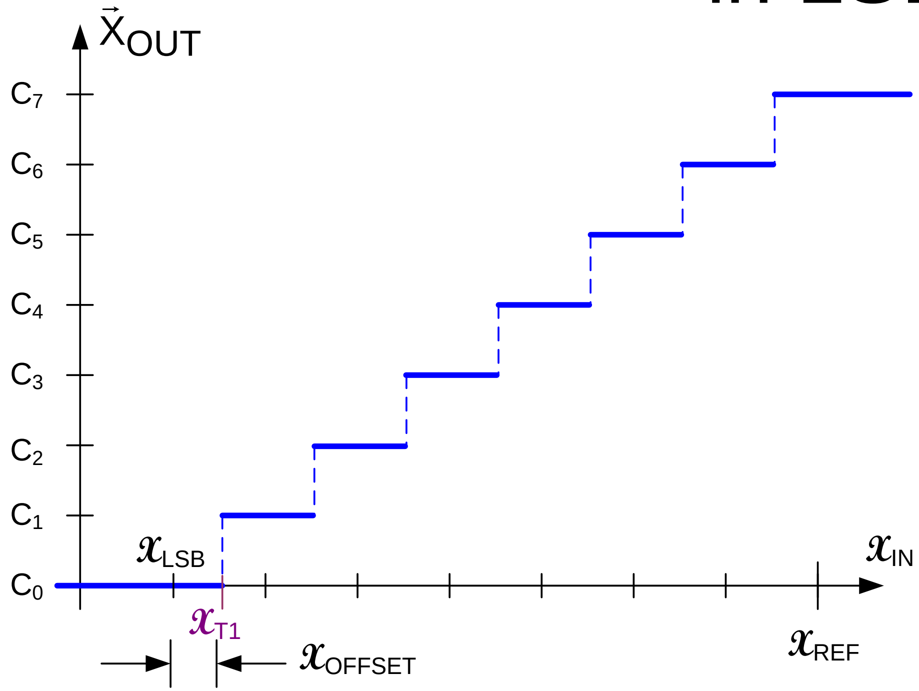
Performance Characterization

Offset

For ADC the offset is (assuming $\mathcal{X}_{LSB}$ is the ideal first transition point)

$\mathcal{X}_{T1} - \mathcal{X}_{LSB}$ - absolute

$$\frac{\mathcal{X}_{T1} - \mathcal{X}_{LSB}}{\mathcal{X}_{LSB}}$$ - in LSB



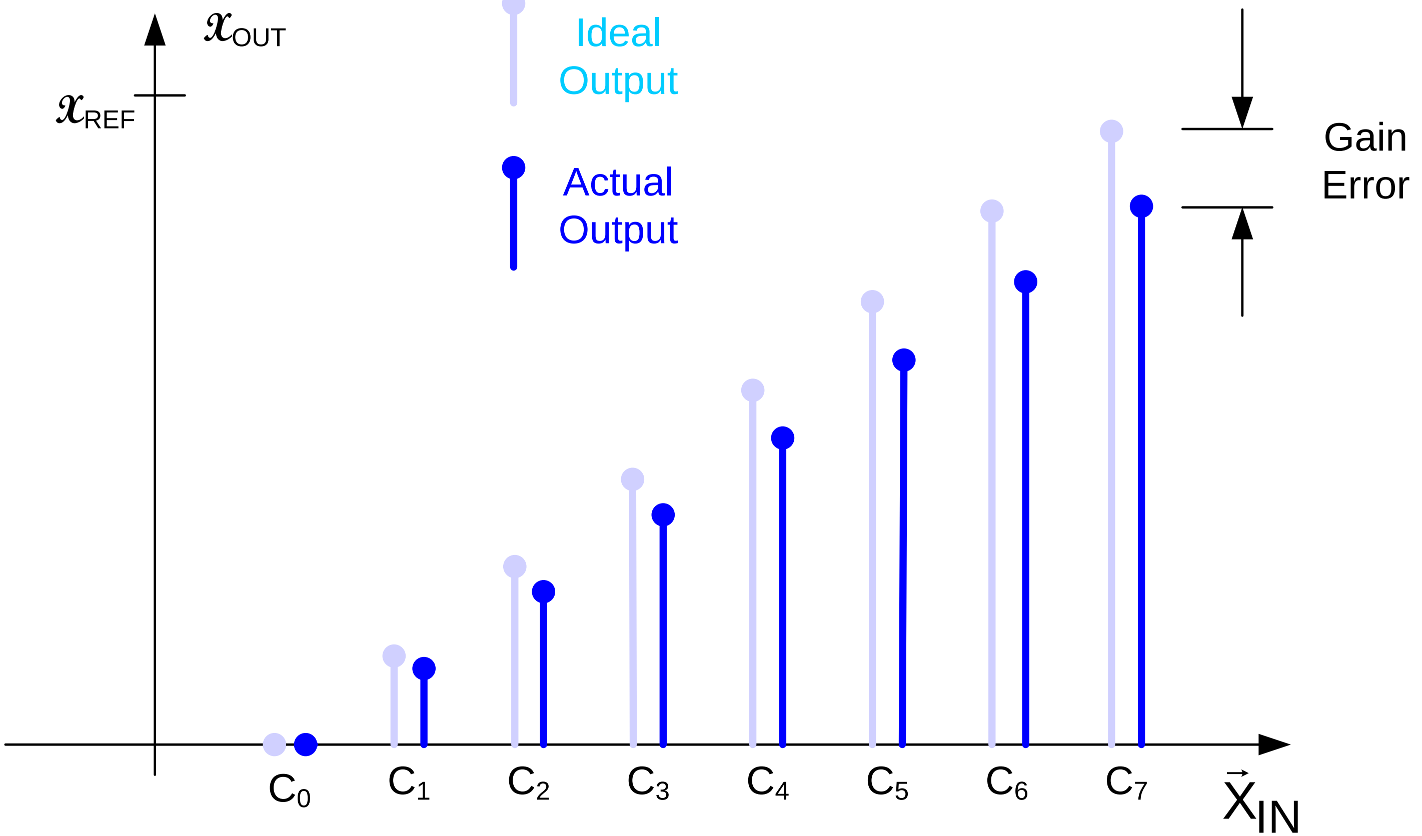
(If ideal first transition point is not $\mathcal{X}_{LSB}$, offset is shift from ideal)

Review from last lecture

Performance Characterization

Gain and Gain Error

For DAC



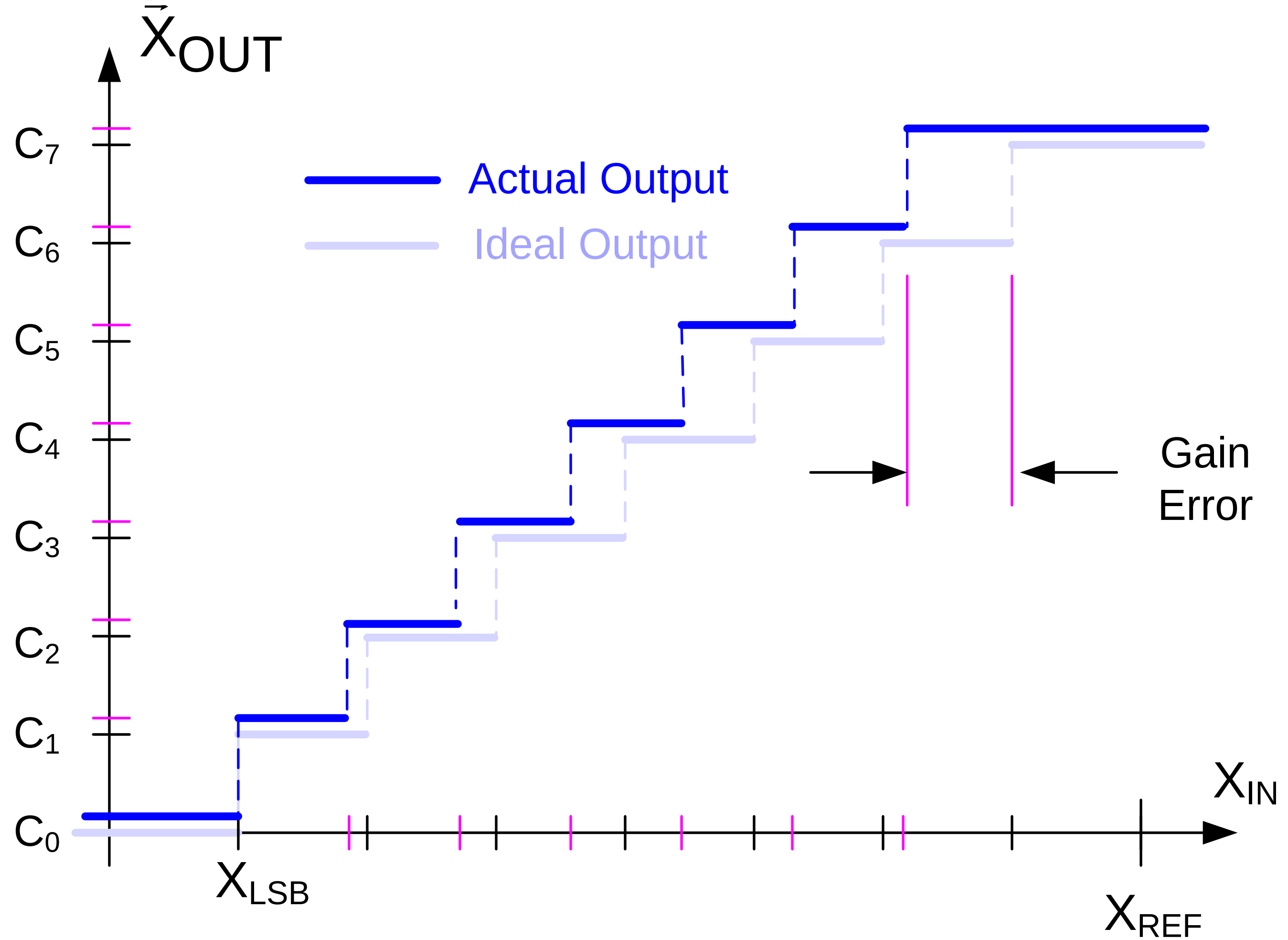
Gain error determined after offset is subtracted from output

Review from last lecture

Performance Characterization

Gain and Gain Error

For ADC

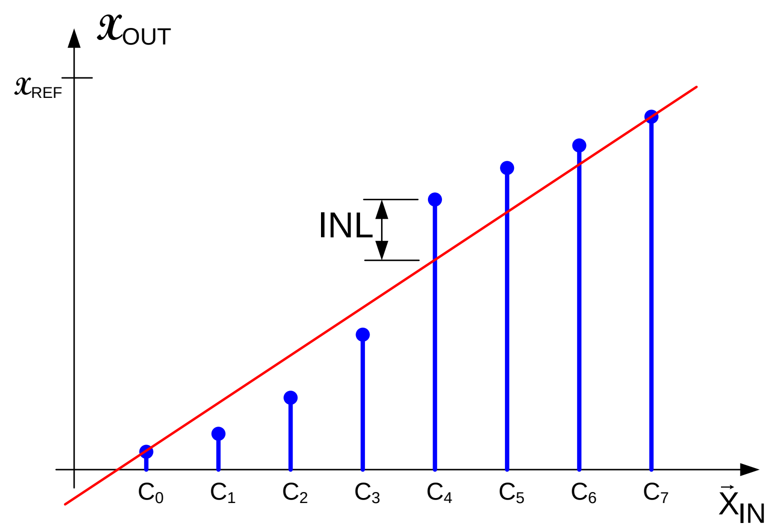


Gain error determined after offset is subtracted from output

Review from last lecture

Integral Nonlinearity (DAC)

Nonideal DAC



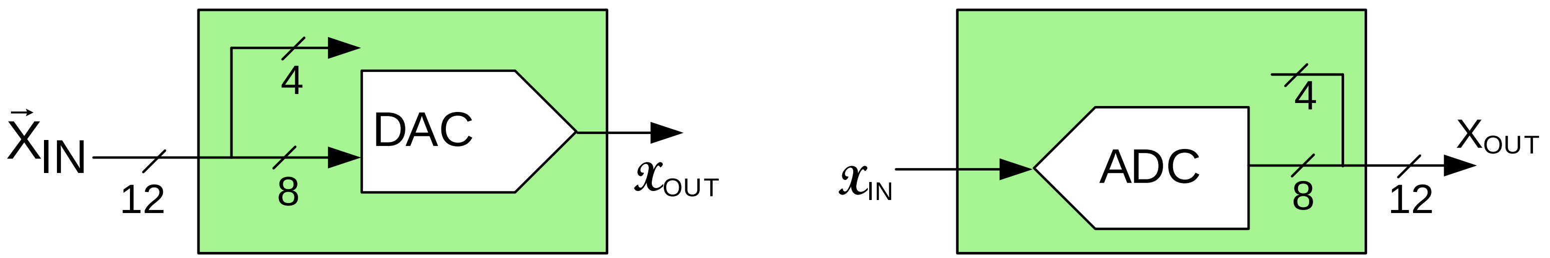
INL often expressed in LSB

$$INL_k = \frac{x_{OUT}(k) - x_{OF}(k)}{x_{LSB}}$$

$$INL = \max_{0 \le k \le N-1} \left\{ \left| INL_k \right| \right\}$$

- INL is often the most important parameter of a DAC
- INL_0 and INL_{N-1} are 0 (by definition)
- There are N-2 elements in the set of INL_k that are of concern
- INL is almost always nominally 0 (i.e. designers try to make it 0)
- INL is a random variable at the design stage
- INL_k is a random variable for $0<k<N-1$
- INL_k and INL_{k+j} are almost always correlated for all k,j (not incl 0, N-1)
- Fit Line is a random variable
- INL is the N-2 order statistic of a set of N-2 correlated random variables

How many bits in this DAC?
How many bits in this ADC?



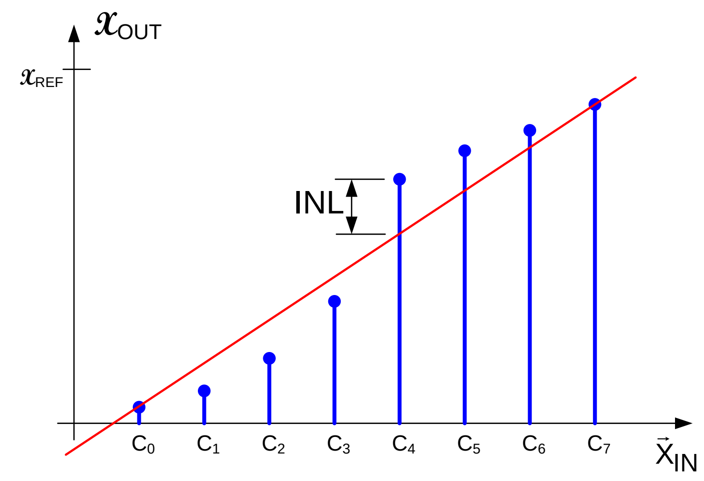
Could even have random number generator generating 4 MSBs in this ADC

Manufacturers can “play games” with characterizing data converters

That is one of the major reasons it is not sufficient to simply specify the number of bits of resolution to characterize data converters !

ENOB of DAC

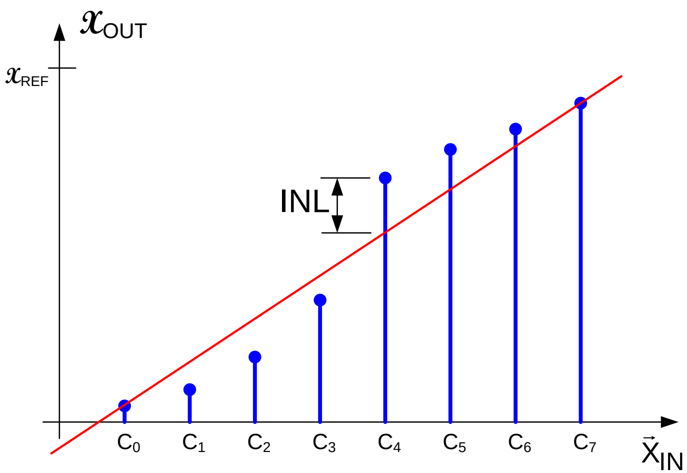
Nonideal DAC



- Concept of Equivalent Number of Bits (ENOB) is to assess performance of an actual DAC to that of an ideal DAC at an “equivalent” resolution level
- Several different definitions of ENOB exist for a DAC
- Here will define ENOB as determined by the actual INL performance
- Will use subscript to define this ENOB, e.g. ENOB_{INL}

ENOB_{INL} of DAC

Nonideal DAC



Premise: A good DAC is often designed so that the INL is equal to ½ LSB. Thus will assume that if an n-bit DAC has an INL of ½ LSB that the ENOB_{INL}=n.

Thus define the effective number of bits, n_{EFF} by the expression

$$\frac{INL}{V_{REF}} = \frac{1}{2} \bullet \frac{1}{2^{n_{EFF}}} = \frac{1}{2^{n_{EFF}+1}} \quad \Longrightarrow \quad n_{EFF} = ENOB_{INL} = \log_2\left(\frac{V_{REF}}{INL}\right) - 1$$

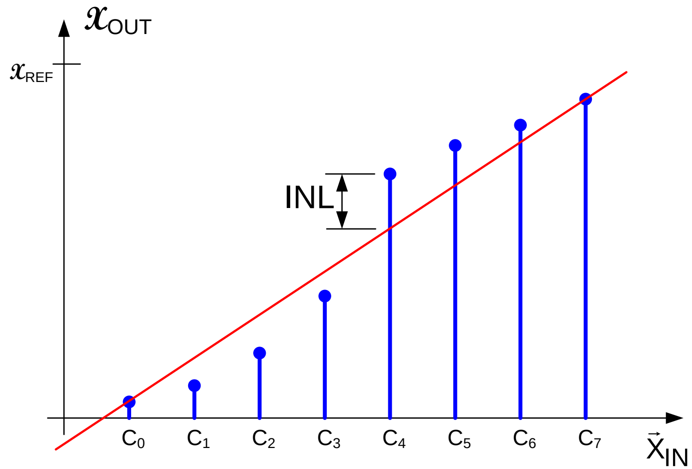
where INL is in volts

Thus, if an n-bit DAC has an INL of ½ LSB

$$ENOB_{INL} = \log_2\left(\frac{V_{REF}}{INL}\right) - 1 = \log_2\left(\frac{2^n V_{LSB}}{\frac{V_{LSB}}{2}}\right) - 1 = \log_2\left(2^{n+1}\right) - 1 = n$$

$ENOB_{INL}$ of DAC

Nonideal DAC



Premise: A good DAC is often designed so that the INL is equal to ½ LSB. Thus will assume that if an n-bit DAC has an INL of ½ LSB that the $ENOB_{INL}$=n.

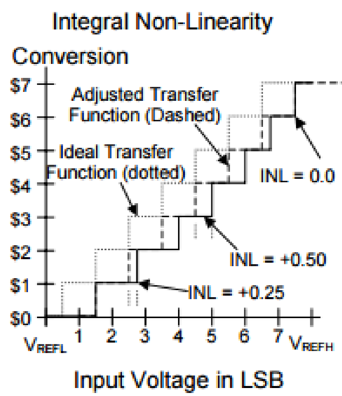
Thus, if an n-bit DAC has an INL of ½ LSB

$$ENOB_{INL} = \log_2\left(\frac{V_{REF}}{INL}\right) - 1 = \log_2\left(\frac{2^n V_{LSB}}{\frac{V_{LSB}}{2}}\right) - 1 = \log_2\left(2^{n+1}\right) - 1 = n$$

Note: With this definition, an n-bit DAC could actually have an $ENOB_{INL}$ larger than n

Integral Nonlinearity (ADC)

Integral Non-Linearity (INL)



Integral Non-Linearity (INL) is defined as the sum from the first to the current conversion (integral) of the non-linearity at each code (*Code DNL*). For example, if the sum of the DNL up to a particular point is 1LSB, it means the total of the code widths to that point is 1LSB greater than the sum of the ideal code widths. Therefore, the current point will convert one code lower than the ideal conversion.

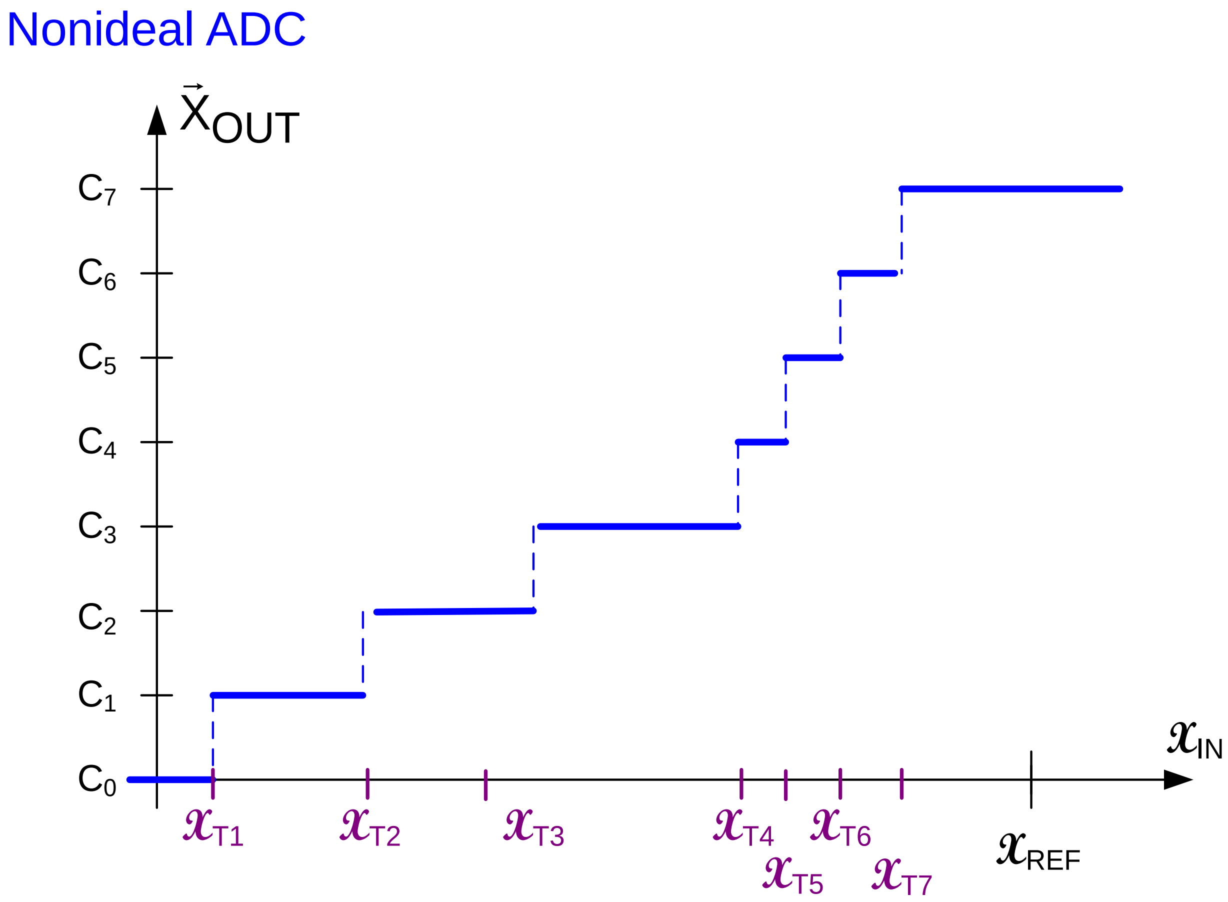
In more fundamental terms, INL represents the curvature in the Actual Transfer Function relative to a baseline transfer function, or the difference between the current and the ideal transition voltages. There are three primary definitions of INL in common use. They all have the same fundamental definition except they are measured against different transfer functions. This fundamental definition is:

Code INL = V(Current Transition) – V(Baseline Transition)

INL = Max(Code INL)

Actually probably more than 3

Integral Nonlinearity (ADC)

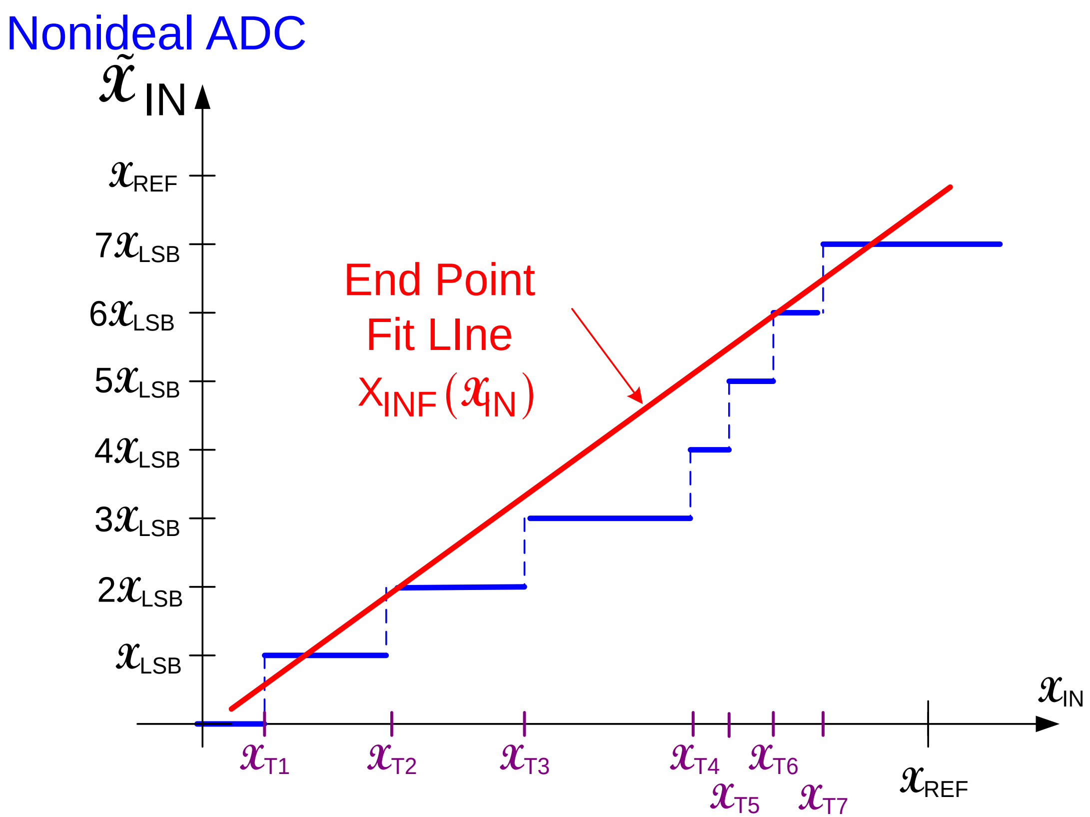


Transition points are not uniformly spaced !

More than one definition for INL exists !

Will give two definitions here

Integral Nonlinearity (ADC)



Consider end-point fit line with interpreted output axis

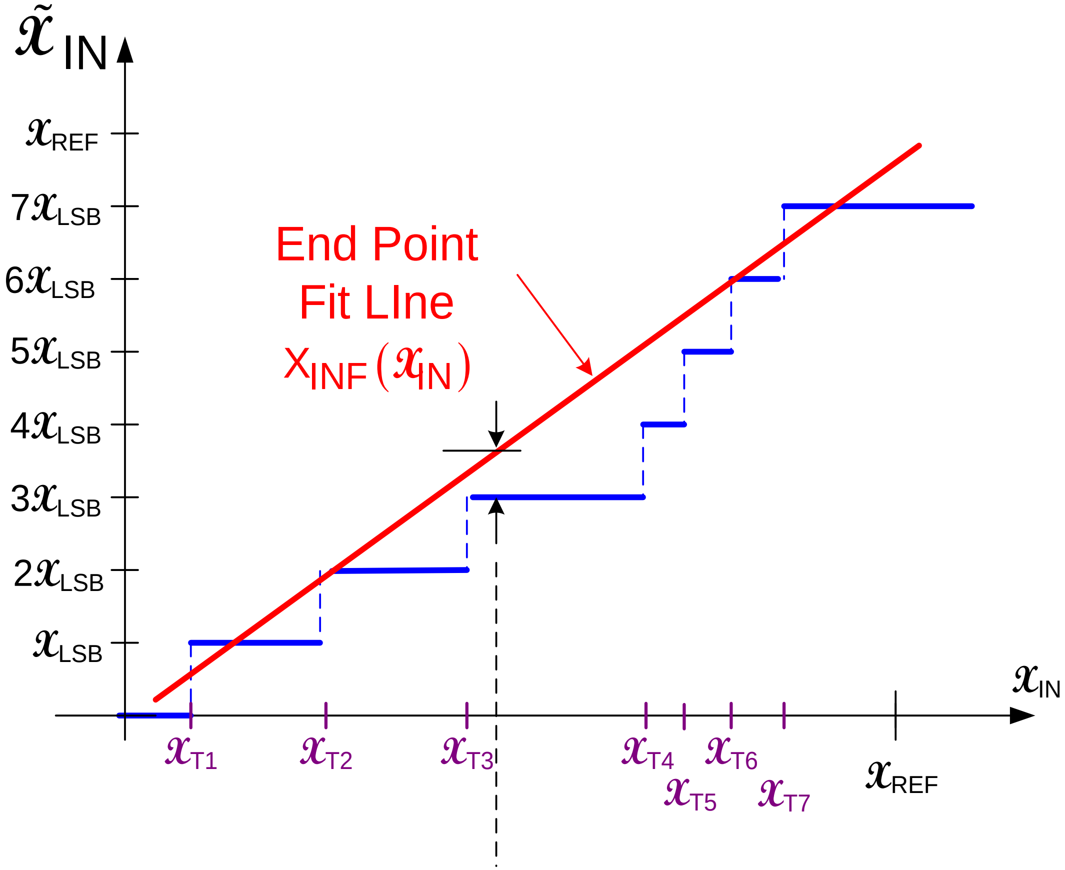
$$X_{INF}(x_{IN}) = m x_{IN} + \left(\frac{x_{LSB}}{2} - m x_{T1}\right)$$

$$m = \frac{(N-2)\,x_{LSB}}{x_{T7} - x_{T1}}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition



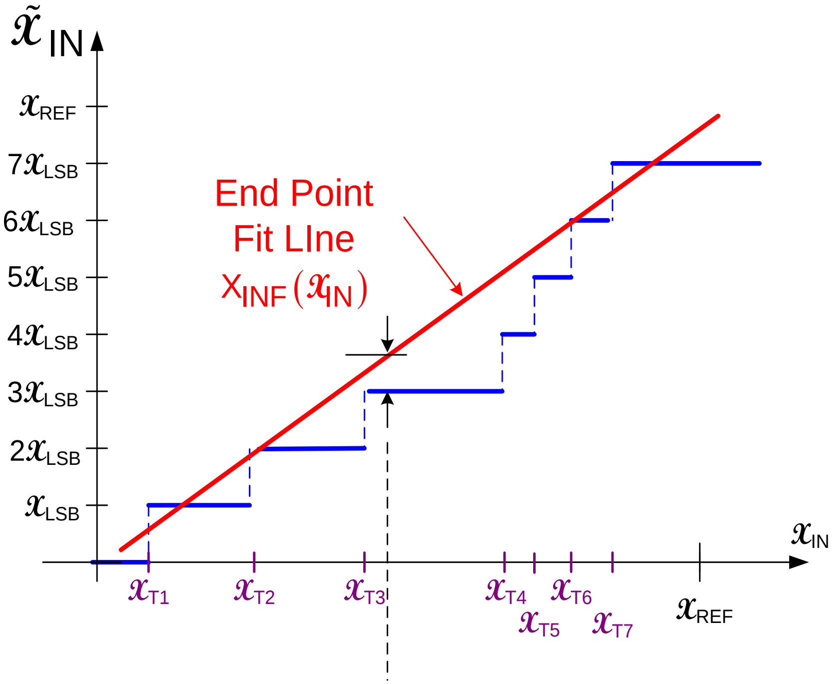
$$INL(x_{IN}) = \tilde{x}_{IN}(x_{IN}) - X_{INF}(x_{IN})$$

$$INL = \max_{0 \le x_{IN} \le x_{REF}} \{ |INL(x_{IN})| \}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Continuous-input based INL definition



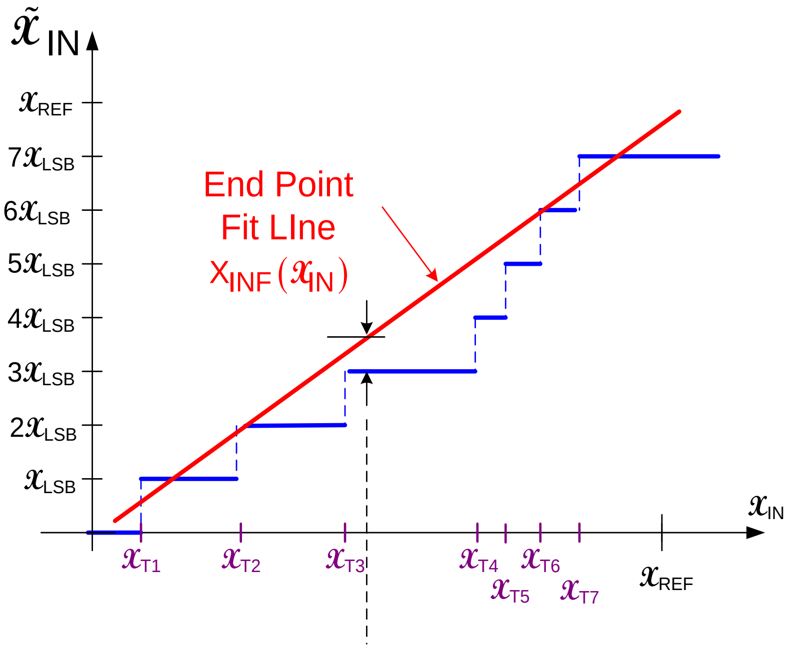
Often expressed in LSB

$$\mathrm{INL}(x_{IN}) = \frac{\tilde{x}_{IN}(x_{IN}) - X_{INF}(x_{IN})}{x_{LSB}}$$

$$\mathrm{INL} = \max_{0 \le x_{IN} \le x_{REF}} \left\{ \left| \mathrm{INL}(x_{IN}) \right| \right\}$$

Integral Nonlinearity (ADC)

Nonideal ADC



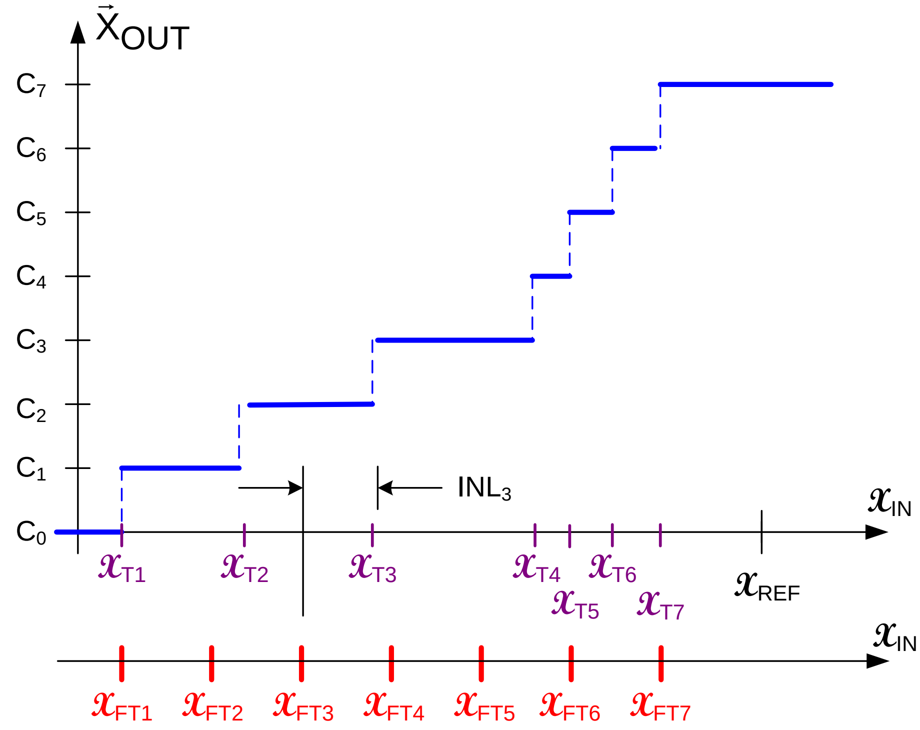
With this definition of INL, the INL of an ideal ADC is $x_{LSB}/2$ (for $x_{T1}=x_{LSB}$)

This is effective at characterizing the overall nonlinearity of the ADC but does not vanish when the ADC is ideal and the effects of the breakpoints are not explicit

Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (most popular)



Place N-3 uniformly spaced points between X_{T1} and $X_{T(N-1)}$ designated x_{FTk}

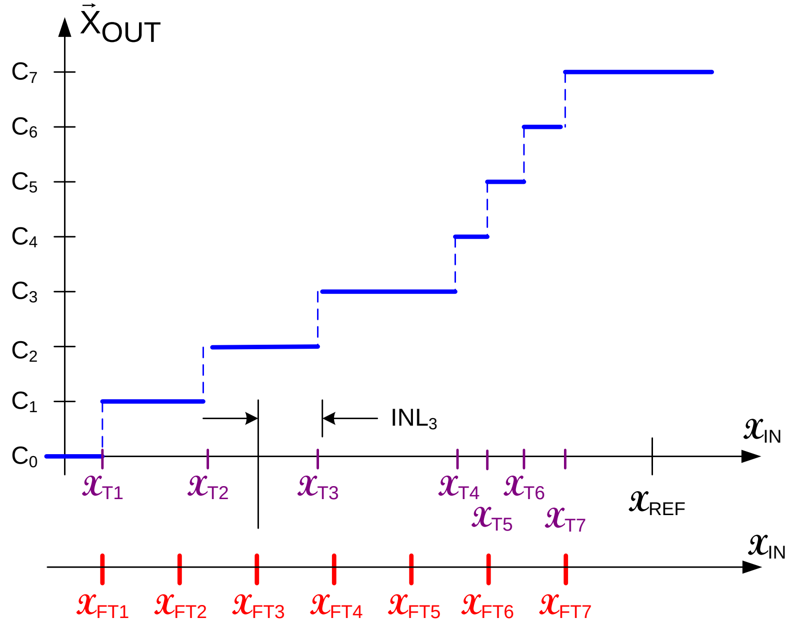
$$INL_k = x_{Tk} - x_{FTk} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \left\{ \left| INL_k \right| \right\}$$

Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition (assuming all break points present)



Often expressed in LSB

$$INL_k = \frac{x_{Tk} - x_{FTl}}{x_{LSB}} \qquad 1 \le k \le N\text{-}2$$

$$INL = \max_{2 \le k \le N-2} \left\{ \left| INL_k \right| \right\}$$

For an ideal ADC, INL is ideally 0

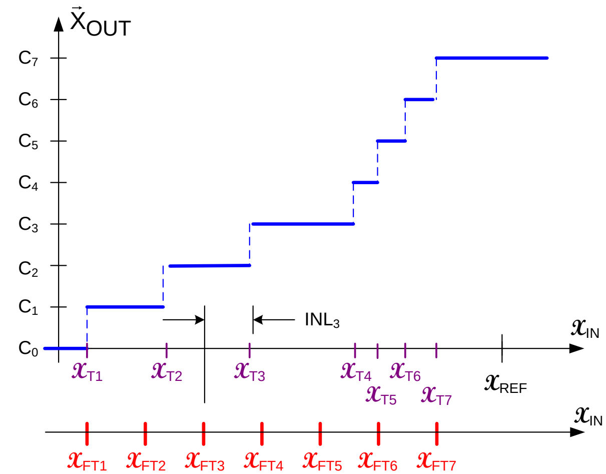
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$INL_k = \frac{x_{Tk} - x_{FTl}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \left\{ \left| INL_k \right| \right\}$$



- INL is often the most important parameter of an ADC
- INL_1 and INL_{N-1} are 0 (by definition)
- There are N-3 elements in the set of INL_k that are of concern
- INL is a random variable at the design stage
- INL_k is a random variable for $0<k<N-1$
- INL_k and INL_{k+j} are correlated for all k,j (not incl 0, N-1) for most architectures
- Fit Line (for cont INL) and uniformly spaced break pts (breakpoint INL) are random variables
- INL is the N-3 order statistic of a set of N-3 correlated random variables (breakpoint INL)

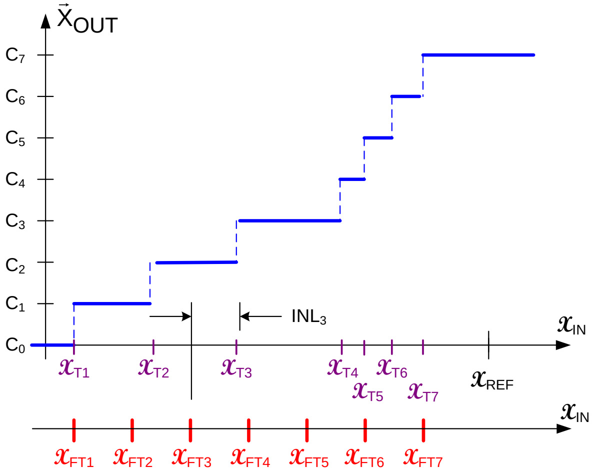
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N\text{-}2$$

$$INL = \max_{2 \le k \le N-2} \{|INL_k|\}$$



- At design stage, INL characterized by standard deviation of the random variable
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - -Model parameters become random variables
  - -Process parameters affect multiple model parameters causing model parameter correlation
  - -Simulation times can become very large

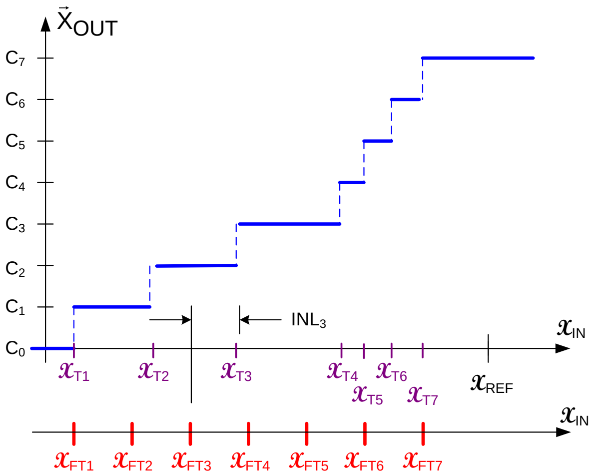
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$\mathrm{INL_k} = \frac{\mathcal{X}_{\mathrm{Tk}} - \mathcal{X}_{\mathrm{FTl}}}{\mathcal{X}_{\mathrm{LSB}}} \qquad 1 \le k \le N-2$$

$$\mathrm{INL} = \max_{2 \le k \le N-2} \left\{ \left| \mathrm{INL_k} \right| \right\}$$



- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- INL is a random variable and is a major contributor to yield loss in many designs
- Expected value of $\mathrm{INL_k}$ at k=(N-1)/2 is largest for many architectures
- This definition does not account for missing transitions
- Major effort in ADC design is in obtaining an acceptable yield

INL-based ENOB

Consider initially the continuous INL definition for an ADC where the INL of an ideal ADC is $X_{LSB}/2$

Assume $$INL = \theta X_{REF} = \upsilon X_{LSBR}$$

where X_{LSBR} is the LSB based upon the defined resolution

Define the effective LSB by
$$\mathcal{X}_{LSBEFF} = \frac{\mathcal{X}_{REF}}{2^{n_{EQ}}}$$

Thus
$$INL = \theta 2^{n_{EQ}} X_{LSBEFF}$$

Since an ideal n-bit ADC has an INL of $X_{LSB}/2$, express INL in terms of ideal ADC
$$INL = \left[\theta 2^{(n_{EQ}+1)}\right]\left(\frac{X_{LSBEFF}}{2}\right)$$

Setting term in [ ] to 1, can solve for n_{EQ} to obtain

$$ENOB = n_{EQ} = \log_2\left(\frac{1}{2\theta}\right) = n_R - 1 - \log_2(\upsilon)$$

where n_R is the defined resolution

INL-based ENOB

$$\text{ENOB} = n_R - 1 - \log_2(\upsilon)$$

Consider an ADC with specified resolution of n_R and INL of v LSB

υ	ENOB
½	n
1	n-1
2	n-2
4	n-3
8	n-4
16	n-5

Performance Characterization of Data Converters

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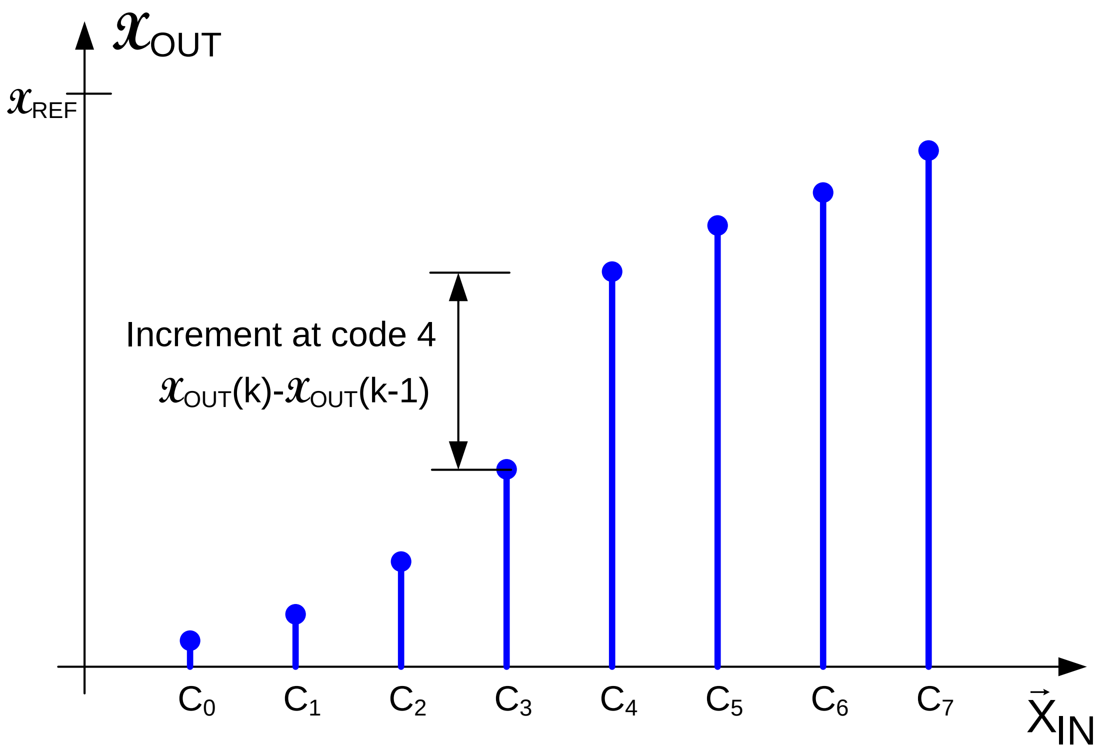
  - Power Dissipation

Differential Nonlinearity (DAC)

Nonideal DAC

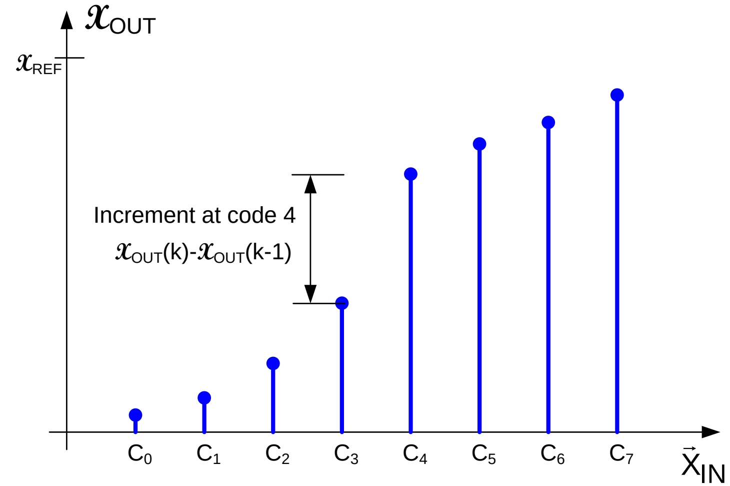


DNL(k) is the actual increment from code (k-1) to code k minus the ideal increment normalized to X_{LSB}

$$\mathrm{DNL}(k)=\frac{X_{OUT}(k)-X_{OUT}(k-1)-X_{LSB}}{X_{LSB}}$$

Differential Nonlinearity (DAC)

Nonideal DAC



Increment at code k is a signed quantity and will be negative if $X_{OUT}(k)<X_{OUT}(k-1)$

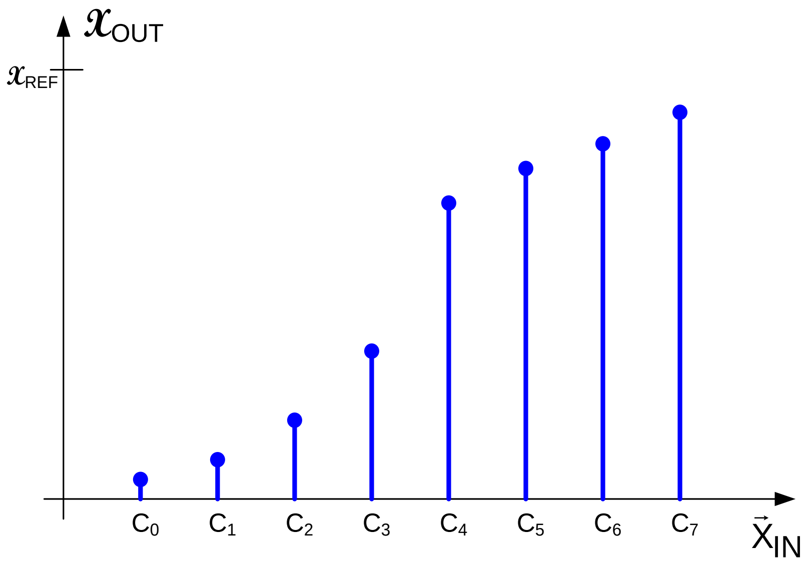
$$DNL(k)=\frac{X_{OUT}(k)-X_{OUT}(k-1)-X_{LSB}}{X_{LSB}}$$

$$DNL=\max_{1\leq k\leq N-1}\left\{\left|DNL(k)\right|\right\}$$

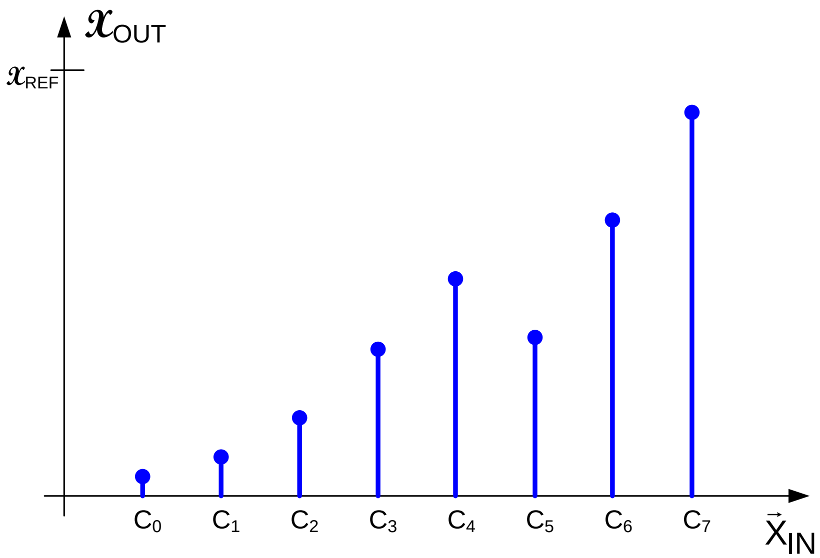
DNL=0 for an ideal DAC

Monotonicity (DAC)

Nonideal DAC



Monotone DAC



Non-monotone DAC

Definition:

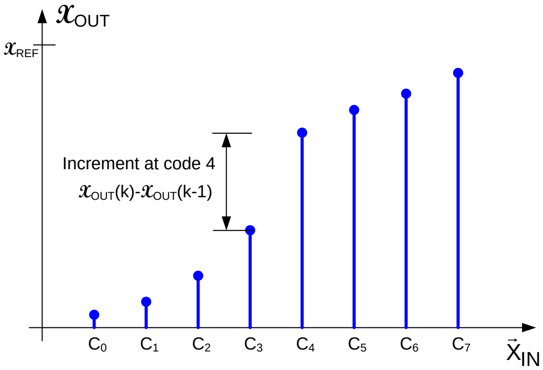
A DAC is monotone if $x_{OUT}(k) > x_{OUT}(k\text{-}1)$ for all k

Theorem:

A DAC is monotone if DNL(k)> -1 for all k

Differential Nonlinearity (DAC)

Nonideal DAC



Theorem: The INL_k of a DAC can be obtained from the DNL by the expression

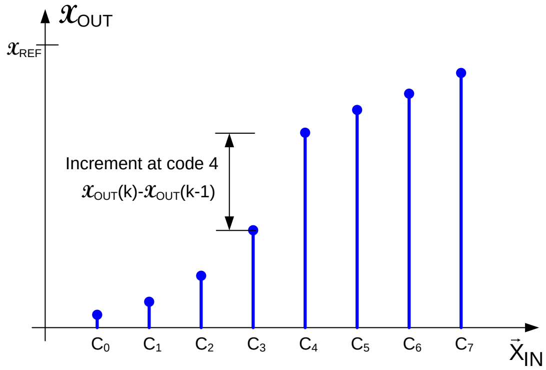
$$INL_k = \sum_{i=1}^{k} DNL(i)$$

Caution: Be careful about using this theorem to measure the INL since errors in DNL measurement (or simulation) can accumulate

Corollary: $DNL(k)=INL_k-INL_{k-1}$

Differential Nonlinearity (DAC)

Nonideal DAC



Theorem: If the INL of a DAC satisfies the relationship

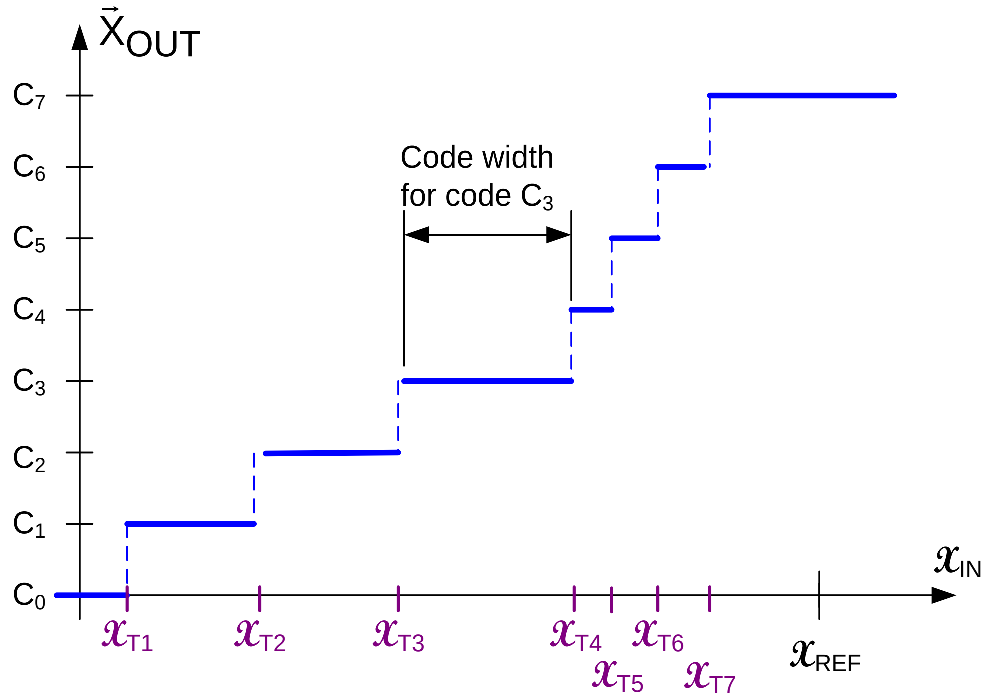
$$\text{INL} < \frac{1}{2}\, X_{LSB}$$

then the DAC is monotone

Note: This is a necessary but not sufficient condition for monotonicity

Differential Nonlinearity (ADC)

Nonideal ADC

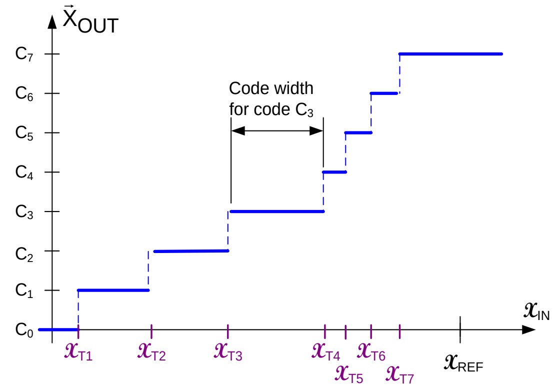


DNL(k) is the code width for code k – ideal code width normalized to X_{LSB}

$$DNL(k) = \frac{x_{T(k+1)} - x_{Tk} - x_{LSB}}{x_{LSB}}$$

Differential Nonlinearity (ADC)

Nonideal ADC



$$\mathrm{DNL}(k)=\frac{x_{T(k+1)}-x_{Tk}-x_{LSB}}{x_{LSB}}$$

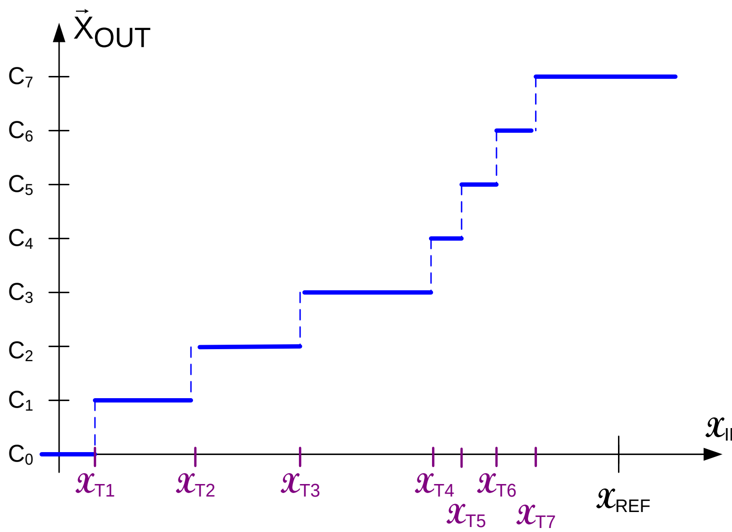
$$\mathrm{DNL}=\max_{2\le k\le N-1}\left\{\left|\mathrm{DNL}(k)\right|\right\}$$

DNL=0 for an ideal ADC

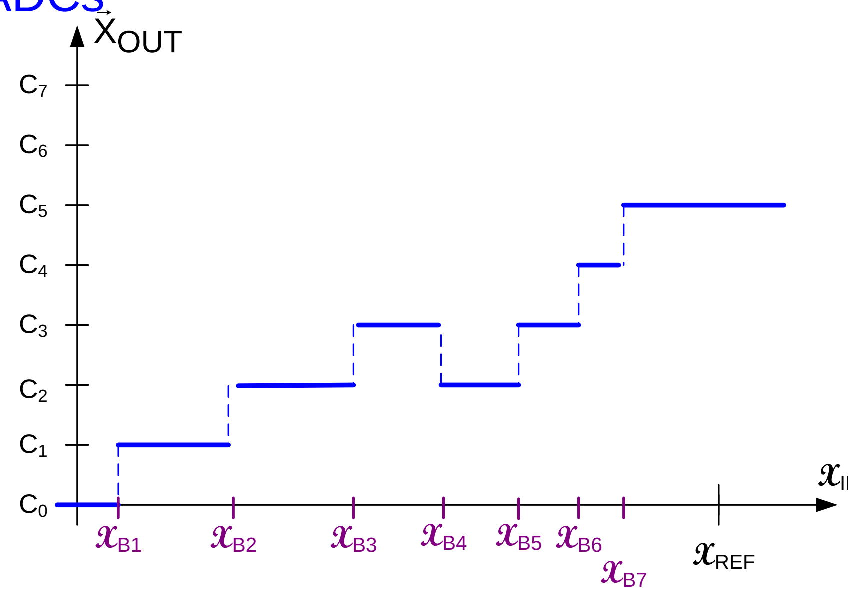
Note: In some nonideal ADCs, two or more break points could cause transitions to the same code C_k making the definition of DNL ambiguous

Monotonicity in an ADC

Nonideal ADCs



Monotone ADC



Nonmonotone ADC

Definition: An ADC is monotone if the

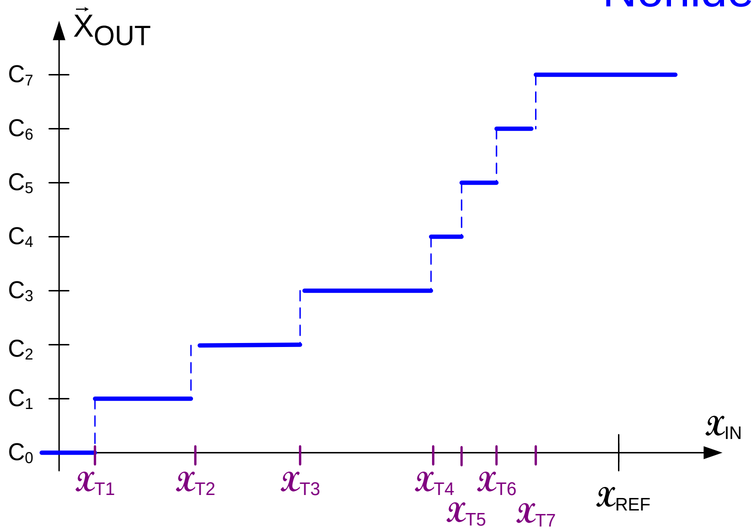
$$\vec{X}_{OUT}(x_k) \geq \vec{X}_{OUT}(x_m) \quad \text{whenever} \quad x_k \geq x_m$$

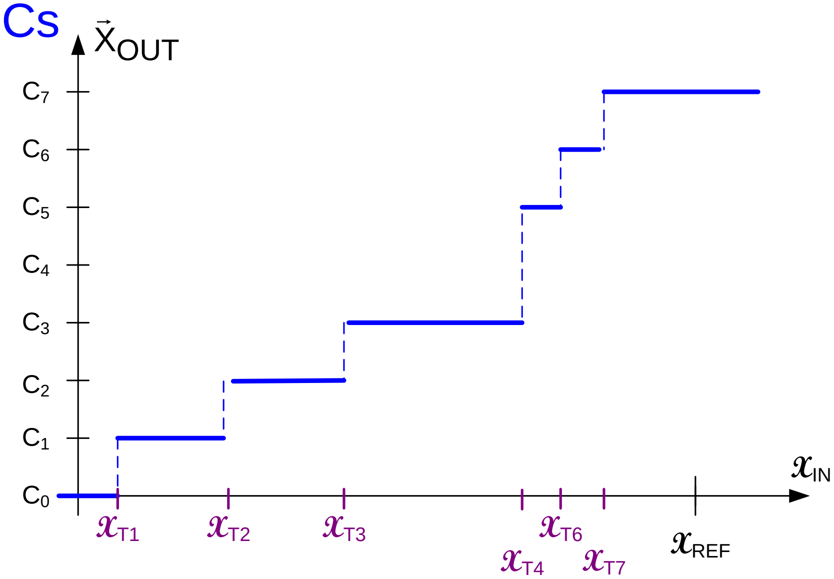
Note: Have used x_{Bk} instead of x_{Tk} since more than one transition point to a given code

Note: Some authors do not define monotonicity in an ADC.

Missing Codes (ADC)

Nonideal ADCs





No missing codes

One missing code

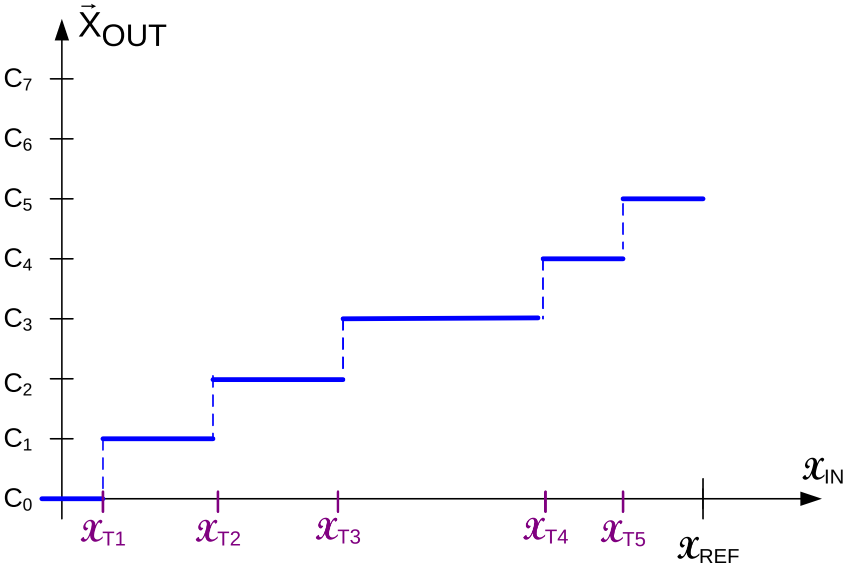
Definition: An ADC has no missing codes if there are N-1 transition points and a single LSB code increment occurs at each transition point. If these criteria are not satisfied, we say the ADC has missing code(s).

Note: With this definition, all codes can be present but we still say it has “missing codes”

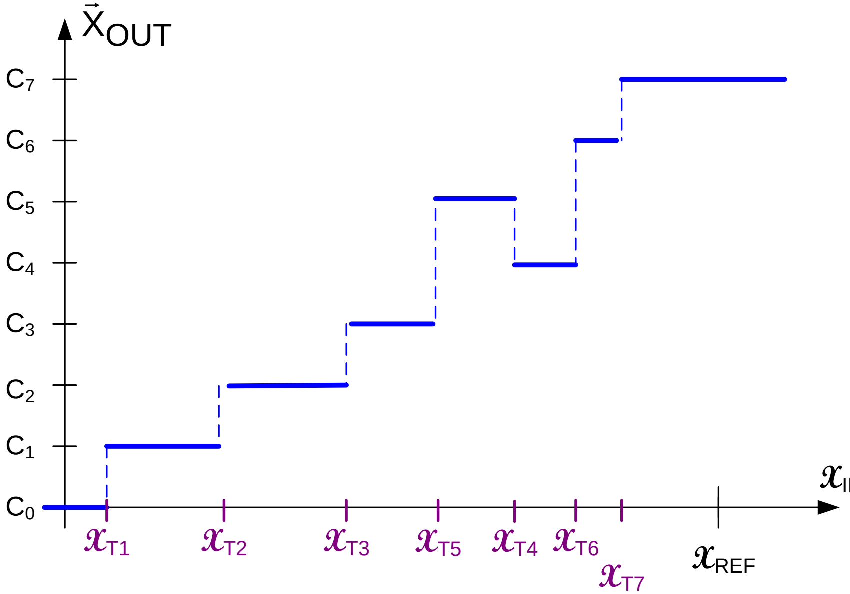
Note: Some authors claim that missing codes in an ADC are the counterpart to nonmonotonicity in a DAC. This association is questionable.

Missing Codes (ADC)

Nonideal ADCs



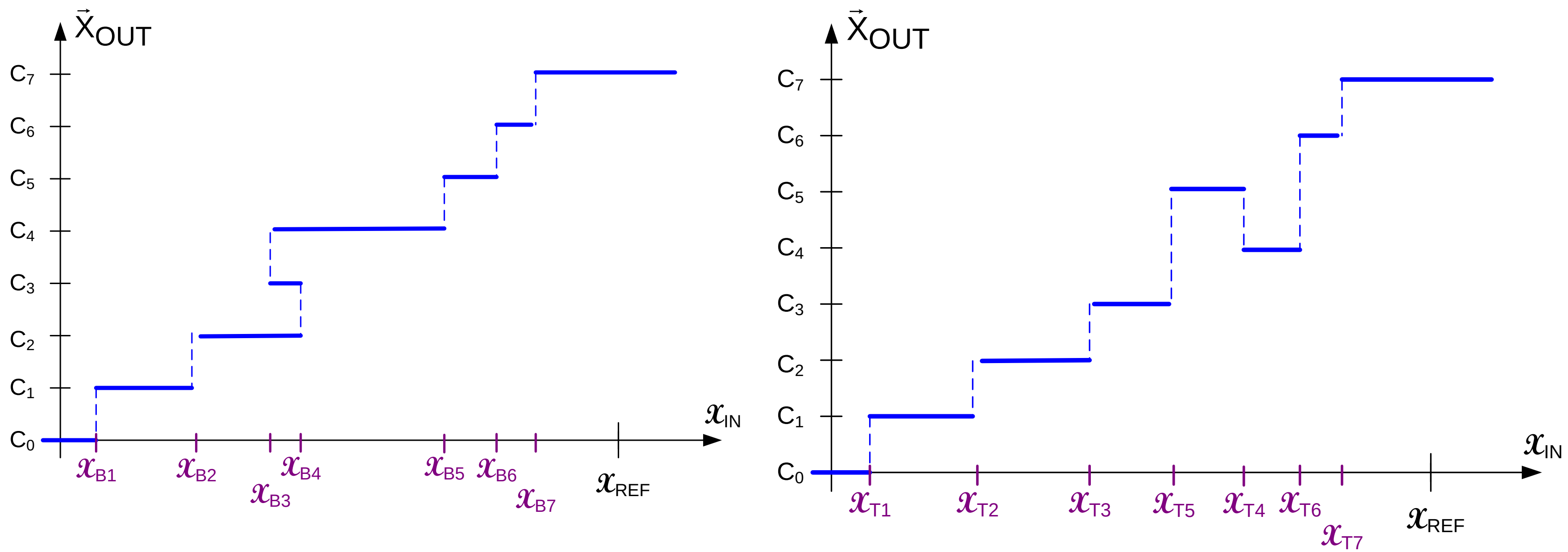
Missing codes



Missing code with all codes present

Weird Things Can Happen

Nonideal ADCs



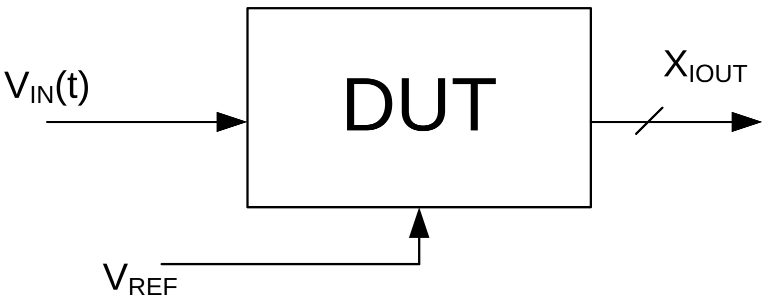
- Multiple outputs for given inputs
- All codes present but missing codes

Be careful on definition and measurement of linearity parameters to avoid having weird behavior convolute analysis, simulation or measurements

Most authors (including manufacturers) are sloppy with their definitions of data converter performance parameters and are not robust to some weird operation

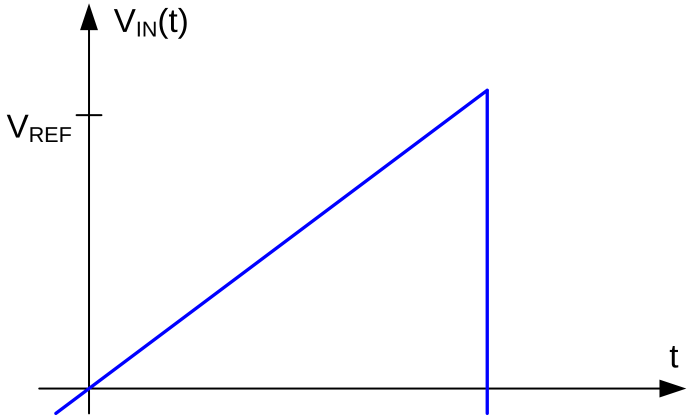
Linearity Measurements (testing)

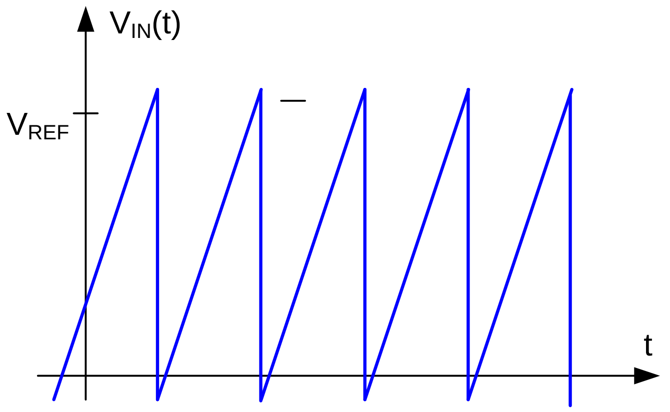
Consider ADC



Linearity testing often based upon code density testing

Code density testing:

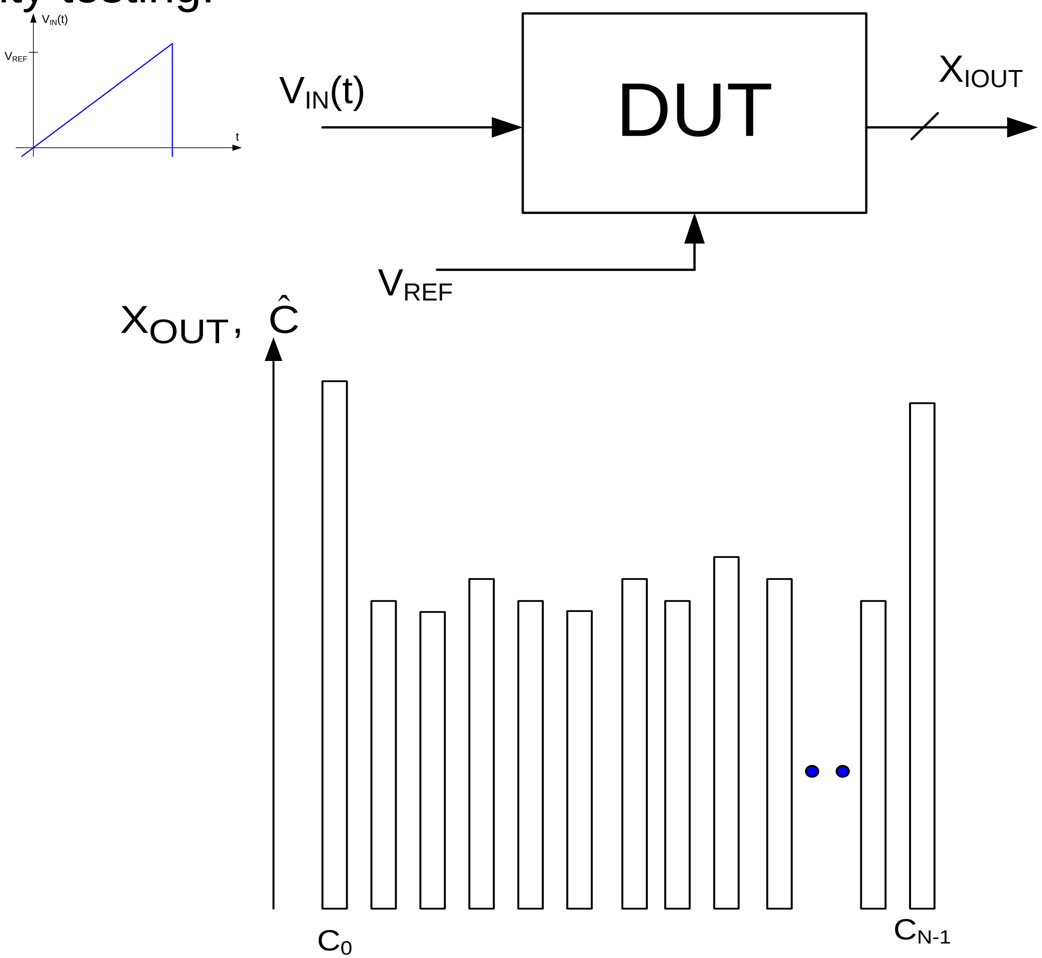




Ramp or multiple ramps often used for excitation
Linearity of test signal is critical (typically 3 or 4 bits more linear than DUT)

Linearity Measurements (testing)

Code density testing:



- First and last bins generally have many extra counts (and thus no useful information)
- Typically average 16 or 32 hits per code

Linearity Measurements (testing)

Code density testing:

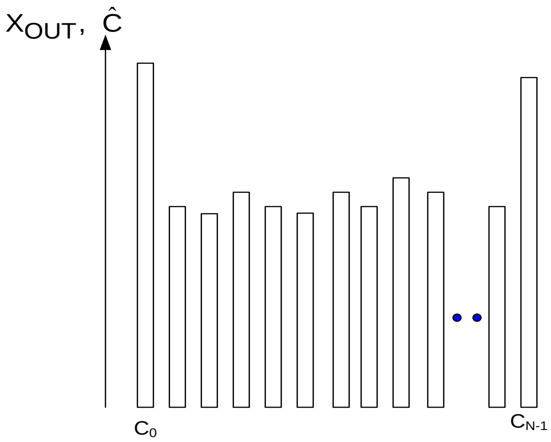
$$\bar{C} = \frac{\sum_{i=1}^{N-2} \hat{C}_i}{N-2}$$

$$DNL_i = \frac{\hat{C}_i - \bar{C}}{\bar{C}}$$

$$INL_i = \begin{cases} 0 & i=0,N-2 \\ \dfrac{\left[\sum_{k=1}^{i} \hat{C}_k\right] - i\bar{C}}{\bar{C}} & 1 \le i \le N-3 \end{cases}$$

$$DNL = \max_{1 \le i \le N-2} \{|DNL_i|\}$$

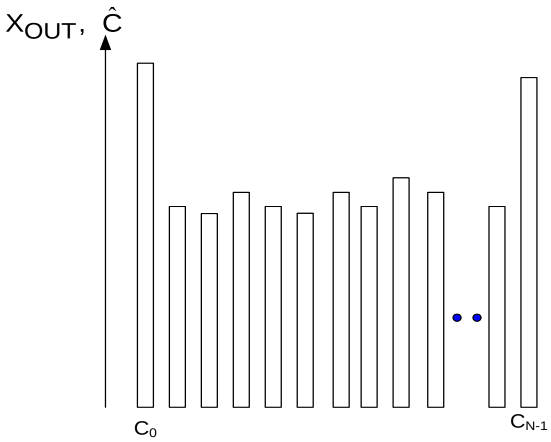
$$INL = \max_{1 \le i \le N-3} \{|INL_i|\}$$



- This measurement is widely used
- Does not keep track of order bins are filled
- Some weird things can occasionally happen with this approach

Linearity Measurements (testing)

Code density testing:



$$\mathrm{DNL} = \max_{1 \le i \le N-2} \left\{ \left| DNL_i \right| \right\}$$

$$\mathrm{INL} = \max_{1 \le i \le N-3} \left\{ \left| INL_i \right| \right\}$$

Though INL and DNL for an ADC are rigorously defined, measuring the actual transition points is not practical even if n is small so code density tests are almost always used to “test” the INL and the DNL

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Linearity

A data converter (ADC or DAC) can be viewed as an amplifier that interfaces between the analog and digital domains

Linearity is of considerable concern in amplifiers irrespective of whether the I/O is analog:analog, analog:digital, digital:analog, or digital:digital

Though INL and DNL give some information about linearity (the term "linearity" is even included in their names!), much information about the actual linearity of a data converter is suppressed in the INL and DNL metrics

The seemingly simple concept of linearity is challenging to accurately characterize

Performance Characterization of Data Converters

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Low-f Spurious Free Dynamic Range (SFDR)
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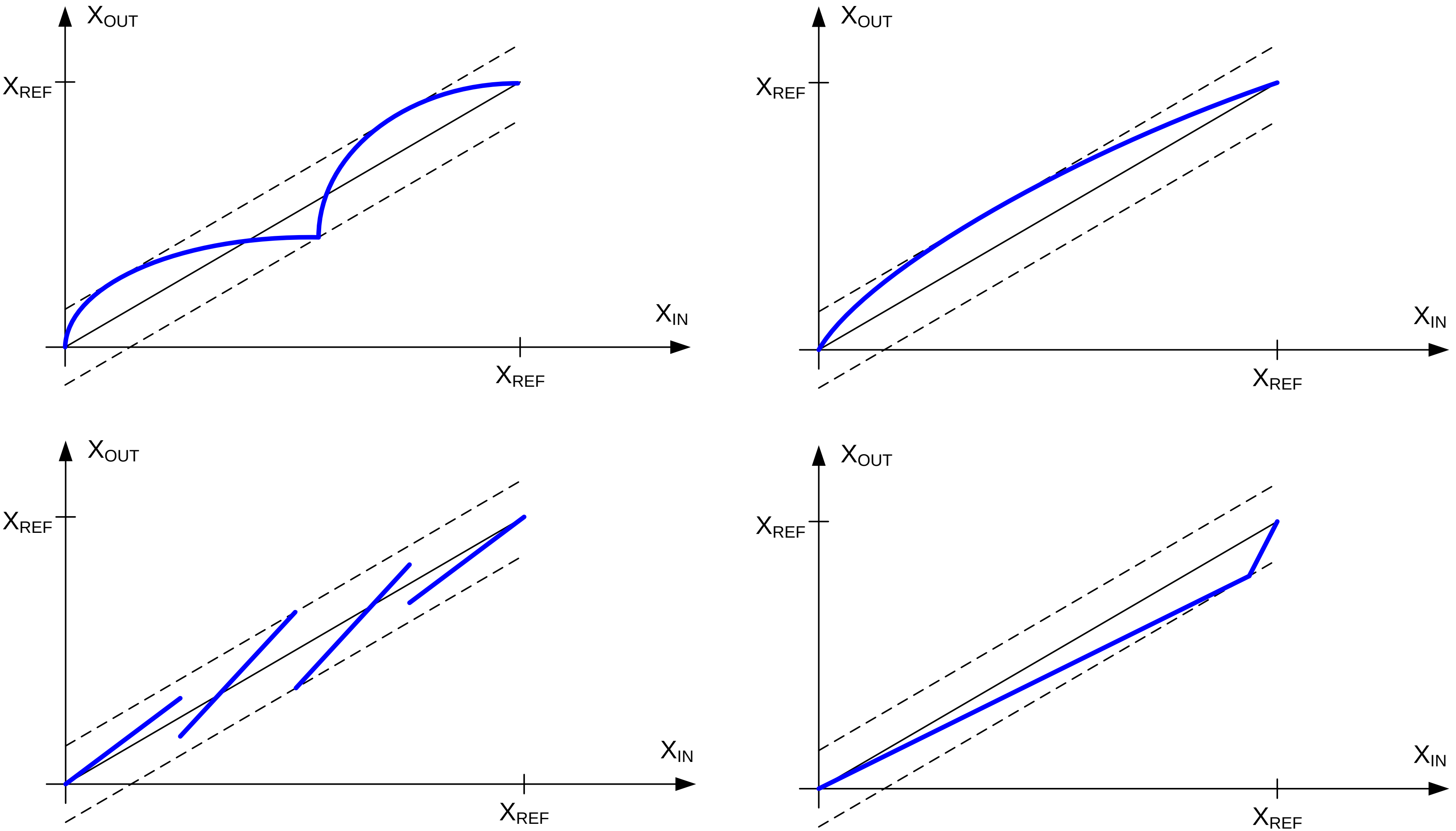
Linearity Metrics

Spectral Characterization

Spectral Characterization

INL Often Not a Good Measure of Linearity

Four identical INL with dramatically different linearity

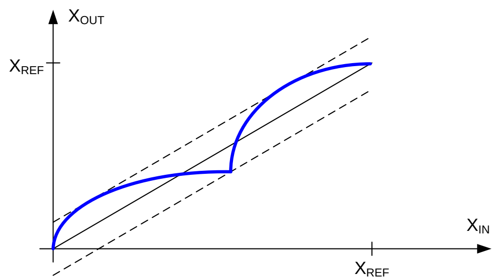


Linearity Issues

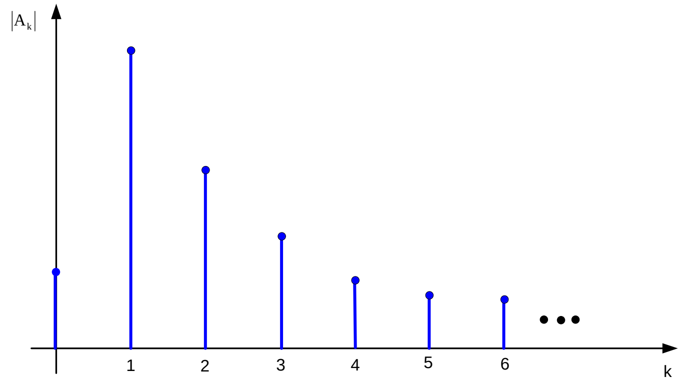
- INL is often not adequate for predicting the linearity performance of a data converter
- Distortion (or lack thereof) is of major concern in many applications
- Distortion is generally characterized in terms of the harmonics that may appear in a waveform when a periodic excitation is applied at the input

Two Popular Methods of Linearity Characterization

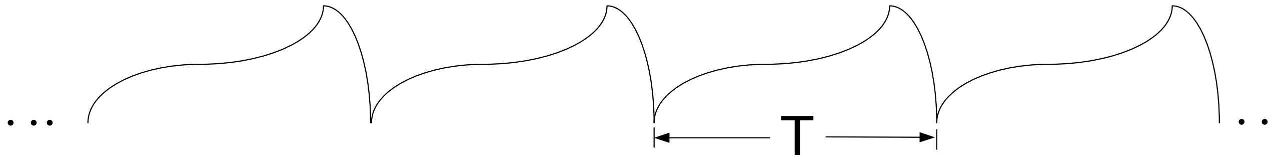
- Integral and Differential *Nonlinearity* *(metrics: INL,* DNL)



- Spectral Characterization (Based upon spectral harmonics of sinusoidal signals   metrics: THD, SFDR, SDR SNR)



Spectral Analysis



If f(t) is periodic

$$f(t) = A_0 + \sum_{k=1}^{\infty} A_k \sin\left(k\omega t + \theta_k\right)$$

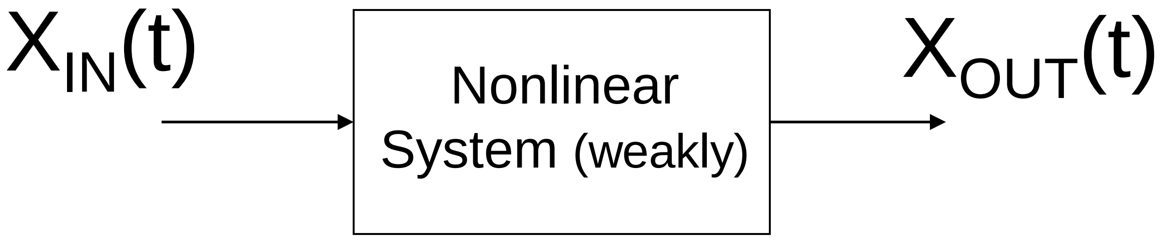
alternately

$$f(t) = A_0 + \sum_{k=1}^{\infty} a_k \sin\left(k\omega t\right) + \sum_{k=1}^{\infty} b_k \cos\left(k\omega t\right) \qquad \omega = \frac{2\pi}{T}$$

$$A_k = \sqrt{a_k^2 + b_k^2}$$

Termed the Fourier Series Representation of f(t)

Spectral Analysis



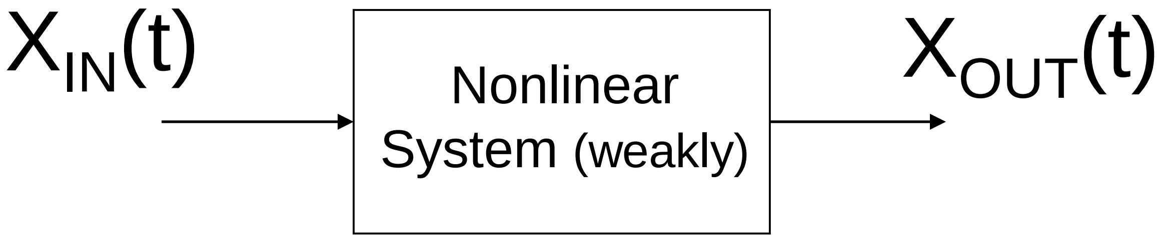
Often the system of interest is ideally linear but practically it is weakly nonlinear.

Often the input is nearly periodic and often sinusoidal and in latter case desired output is also sinusoidal

Weak nonlinearity will cause harmonic distortion (often just termed distortion) of signal as it is propagated through the system

Spectral analysis often used to characterize effects of the weak nonlinearity

Spectral Analysis



Distortion Types:

Frequency Distortion

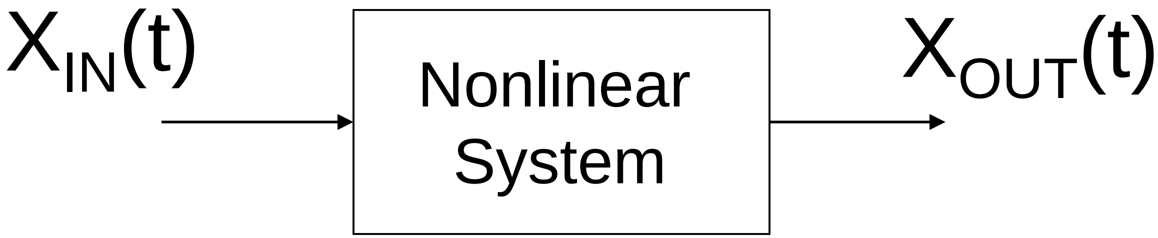
Nonlinear Distortion (alt. harmonic distortion)

Frequency Distortion: Amplitude and phase of system is altered but output is linearly related to input

Nonlinear Distortion: System is not linear, frequency components usually appear in the output that are not present in the input

Spectral Analysis is the characterization of a system with a periodic input with the Fourier series relationships between the input and output waveforms

Spectral Analysis



If $\quad X_{IN}(t) = X_m \sin(\omega t + \theta)$

$$X_{OUT}(t) = A_0 + \sum_{k=1}^{\infty} A_k \sin(k\omega t + \theta_k)$$

All spectral performance metrics depend upon the sequences $\left\langle A_k \right\rangle_{k=0}^{\infty} \quad \left\langle \theta_k \right\rangle_{k=1}^{\infty}$

Spectral performance metrics of interest: SNDR, SDR, THD, SFDR, IMOD

Alternately

$$X_{OUT}(t) = A_0 + \sum_{k=1}^{\infty} a_k \sin(k\omega t) + \sum_{k=1}^{\infty} b_k \cos(k\omega t) \qquad A_k = \sqrt{a_k^2 + b_k^2} \qquad \theta_k = \tan^{-1}\left(\frac{b_k}{a_k}\right)$$

Stay Safe and Stay Healthy !

End of Lecture 26